

IM6103 CMOS Parallel Input-Output Port (PIO)

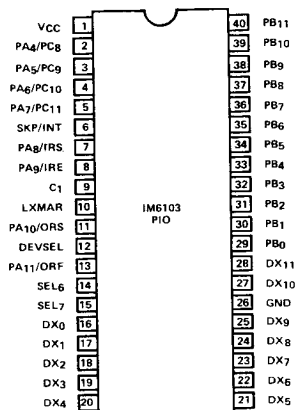
FEATURES

- 20 Programmable I/O Pins
- TTL Compatible Inputs and Outputs
- Compatible with IM6100 Microprocessor Family
- Low Power Dissipation < 10 mW
- Extended Temperature Range, -55°C to +125°C
- Single Power Supply, 4 – 11 Volts

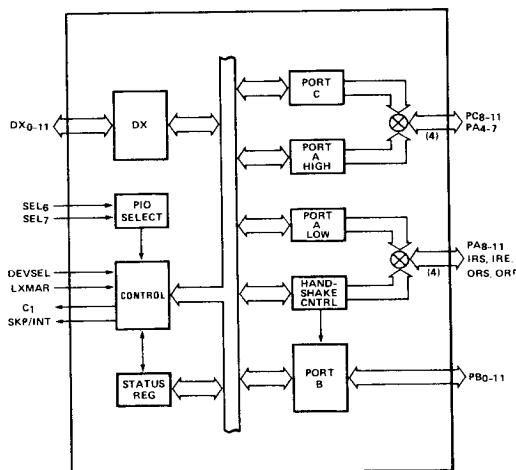
GENERAL DESCRIPTION

The IM6103 is a Parallel Input-Output Port (PIO) device designed for use in IM6100 microcomputer systems. Its function is to provide a general purpose parallel I/O component to interface peripheral equipment to the IM6100 system bus. The functional configuration of the IM6103 is programmed by the user software so that normally no external logic is necessary to interface a wide variety of peripheral devices such as displays, printers, keyboards, etc. to an IM6100 microcomputer system.

A general purpose all-CMOS microcomputer system with 64 x 12 RAM, 1k x 12 ROM and 20 I/O lines can be built with just four CMOS LSI devices — IM6100 microprocessor, IM6512 (64 x 12) RAM, IM6312 (1k x 12) ROM and IM6103 PIO.

PIN CONFIGURATION (outline dwg DL, PL)

BLOCK DIAGRAM



ORDERING INFORMATION

ORDER CODE	IM6103-1	IM6103A	IM6103
PLASTIC PKG	IM6103-1PL	IM6103-A1PL	IM6103-1PL
CERAMIC PKG	IM6103-1DL	IM6103-A1DL	IM6103-1DL
MILITARY TEMP.	IM6103-1MDL	IM6103-AMD1	—
MILITARY TEMP. WITH 883B	IM6103-1MD/ MDL/883B	IM6103-AMD/ 883B	—

IM6103

ABSOLUTE MAXIMUM RATINGS

Operating Temperature -40°C to +85°C
 Industrial IM61031.I -65°C to +150°C
 Storage Temperature +12V
 Supply Voltage -0.3V to V_{CC} +0.3V
 Voltage on Any Input or Output Pin With Respect to GND

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = Industrial

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V _{IH}	Logical "1" Input Voltage		V _{CC} -1.7			V
2	V _{IL}	Logical "0" Input Voltage				0.8	V
3	I _{IL}	Input Leakage	0V ≤ V _{IN} ≤ V _{CC}	-1.0		1.0	μA
4	V _{OH}	Logical "1" Output Voltage	I _{OUT} = 0 except pins 6, 9	V _{CC} -1.0			V
5	V _{OL}	Logical "0" Output Voltage	I _{OUT} = 0			0.45	V
6	I _{OLK}	Output Leakage	0V ≤ V _O ≤ V _{CC}	-1.0		1.0	μA
7	I _{CC}	Supply Current	V _{CC} = 5V C _L = 50 pF; T _A = 25°C F _{CLOCK} = Operating Frequency			2.5	mA
8	C _{IN}	Input Capacitance			7.0	8.0	pF
9	C _O	Output Capacitance			8.0	10.0	pF

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -40°C to +85°C, C_L = 50pF, All times in ns.

	SYMBOL	PARAMETER		MIN	MAX	UNITS
1	t _{adds}	Address Set-Up Time	DX-LXMAR↓			ns
2	t _{addh}	Address Hold Time	LXMAR↓-DX	150		
3	t _{den}	Output Enable Time	DEVSEL↓-DX		550	
4	t _{dc}	Output Enable Time	DEVSEL↓-C ₁		550	
5	t _{dl}	Output Enable Time	DEVSEL↓-SKP		400	
6	t _{ds}	Data Set-Up Time	DX-DEVSEL↑	200		
7	t _{dh}	Data Hold Time	DEVSEL↑-DX	150		
8	t _{ps}	Data In Set-Up Time	Port Data In-LXMAR↓	200		
9	t _{ph}	Data In Hold Time	LXMAR↓-Port Data In	225		
10	t _{d1}	Delay Time	DEVSEL↑-Port Data Out		550	
11	t _{bs}	Data In Set-Up Time	Port B In-IRS↓	200		
12	t _{bh}	Data In Hold Time	IRS↓-Port B In	150		
13	t _{d2}	Output Enable Time	ORS↑-Port B Out		550	
14	t _{d2}	Output Disable Time	ORS↓-Port B Out		200	
15	t _{d3}	Delay Time	IRS↓-IRE↓ ORS↓-ORF↓ DEVSEL↑-IRE↑ DEVSEL↑-ORF↑		550	

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	-40°C to +85°C
Industrial IMM6103I	-65°C to +150°C
Storage Temperature	+8V
Supply Voltage	-0.3V to V _{CC} +0.3V
Voltage on Any Input or Output Pin With Respect to GND	

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = Industrial

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V _{IH}	Logical "1" Input Voltage		V _{CC} -1.7			V
2	V _{IL}	Logical "0" Input Voltage				0.8	V
3	I _{IL}	Input Leakage	0V ≤ V _{IN} ≤ V _{CC}	-1.0		1.0	μA
4	V _{OH}	Logical "1" Output Voltage	I _{OH} = -0.2 mA except pins 6,9	V _{CC} -1.0			V
5	V _{OL}	Logical "0" Output Voltage	I _{OL} = 2.0 mA			0.45	V
6	I _{OLK}	Output Leakage	0V ≤ V _O ≤ V _{CC}	-1.0		1.0	μA
7	I _{CC}	Supply Current	V _{CC} = 5.0V C _L = 50 pF; T _A = 25°C F _{CLOCK} = Operating Frequency			2.5	mA
8	C _{IN}	Input Capacitance			7.0	8.0	pF
9	C _O	Output Capacitance			8.0	10.0	pF

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -40°C to +85°C, C_L = 50pF, All times in ns.

	SYMBOL	PARAMETER		MIN	MAX	UNITS
1	t _{adds}	Address Set-Up Time	DX-LXMAR↓	80		ns
2	t _{addh}	Address Hold Time	LXMAR↓-DX	100		
3	t _{den}	Output Enable Time	DEVSEL↓-DX		450	
4	t _{dc}	Output Enable Time	DEVSEL↓-C ₁		450	
5	t _{di}	Output Enable Time	DEVSEL↓-SKP		330	
6	t _{ds}	Data Set-Up Time	DX-DEVSEL↑	150		
7	t _{dh}	Data Hold Time	DEVSEL↑-DX			
8	t _{ps}	Data In Set-Up Time	Port Data In-LXMAR↓	150		
9	t _{ph}	Data In Hold Time	LXMAR↓-Port Data In			
10	t _{d1}	Delay Time	DEVSEL↑-Port Data Out			
11	t _{bs}	Data In Set-Up Time	Port B in-IRS↓			
12	t _{bh}	Data In Hold Time	IRS↓-Port B In	100		
13	t _{d2}	Output Enable Time	ORS↑-Port B Out		450	
14	t _{d2}	Output Disable Time	ORS↓-Port B Out		200	
15	t _{d3}	Delay Time	IRS↓-IRE↓ ORS↓-ORF↓ DEVSEL↑-IRE↑ DEVSEL↑-ORF↑		450	

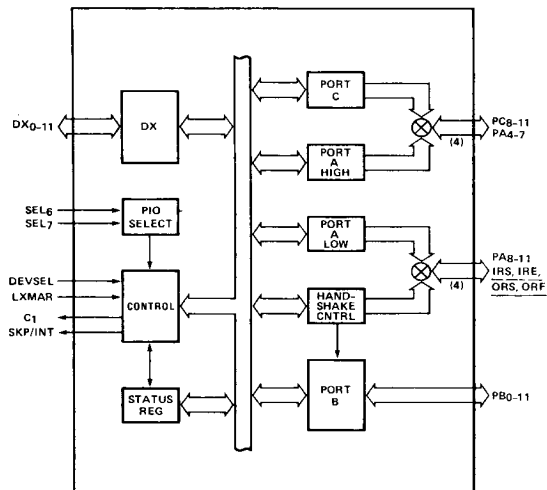


FIGURE 1: Functional Block Diagram.

IM6103 FUNCTIONAL PIN DEFINITION

PIN NUMBER	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
1	VCC		Positive Power Supply
2	PA4	I/O	Port A I/O Line (4). Most Significant Bit of Port A in Mode 10.
	PC8	I/O	Port C I/O Line (8) in Mode 11/OX—Most Significant Bit.
3 ~ 5	PA6 ~ PA4	I/O	Port A5 ~ A7 (Mode 10).
	PC10 ~ PC8	I/O	Port C9 ~ C11 (Mode 11/OX).
6	SKP/INT	O	Time Multiplexed SKP and INTREQ lines to the IM6100 Microprocessor — Active Low.
7	PA8	I/O	Port A I/O Line in Mode 11/10 — Most Significant Bit of Port A in Mode 11.
	IRS	O	Input Register Strobe to clock data into Port B in Handshake Mode (Mode OX). Port B Latches in the data on the falling edge of IRS (IRS↓).
8	PA9	I/O	Port A9 (Mode 11/10).
	IRE	O	Input Register Empty output goes high when Port B input buffer has been read by the IM6100 microprocessor. It goes low when Port B input buffers are strobed in by IRS↓. (Mode OX). PIO may be programmed to generate an INTREQ on IRE↓.

IM6103 FUNCTIONAL PIN DEFINITION (Continued)

PIN NUMBER	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
9	C ₁	O	C ₁ output goes low upon completion of PIO Port data transfer to the IM6100 Accumulator (AC). This output is an open-drain output to be wire-OR'D with C ₁ Lines from other IM6100 peripheral controllers.
10	LXMAR	I	Address Latch enable signal from the IM6100. PIO clocks in address and control information from the IM6100 on the falling edge of LXMAR (LXMAR↓). All Port inputs are sampled at LXMAR↓.
11	PA ₁₀	I/O	Port A ₁₀ (Mode 11/10).
	ORS	I	Output Register Strobe input to enable Port B output buffers in Mode OX. Port B is tri-stated when ORS is low.
12	DEVSEL	I	Input-Output Device Select control line from the IM6100. It performs both the read and write function. The first negative transition after LXMAR↓, enables the DX output buffers of the selected PIO for a 'read' operation. When DEVSEL returns high, the 'read' operation is terminated. The second negative-going pulse on DEVSEL serves as a 'write' pulse to the selected PIO and the IM6100 AC data is written into the selected PIO register or port on the rising edge.
13	PA ₁₁	I/O	Port A ₁₁ (Mode 11/10)—Least Significant bit of Port A.
	ORF	O	Output Register Full output goes high when the IM6100 writes into Port B in a handshake mode. It goes low when the peripheral device reads Port B by enabling ORS high. The PIO may be programmed to generate an INTREQ on ORF↓ (Mode OX).
14	SEL ₆	I	A Chip Select Input. PIO has two chip selects, SEL ₆ and SEL ₇ , thereby enabling up to four PIO chips in a system.
15	SEL ₇	I	A Chip Select Input.
16 ~ 25	DX ₀ ~ DX ₉	I/O	The IM6100 System bus (Data and Address).
26	GND		Ground
27 ~ 28	DX ₁₀ ~ DX ₁₁	I/O	IM6100 System bus (Data and Address).
29 ~ 40	PB ₀ ~ PB ₁₁	I/O	I/O Port Pin. PB ₀ is the most significant bit, and PB ₁₁ is the least significant bit.

IM6100 SYSTEM TIMING

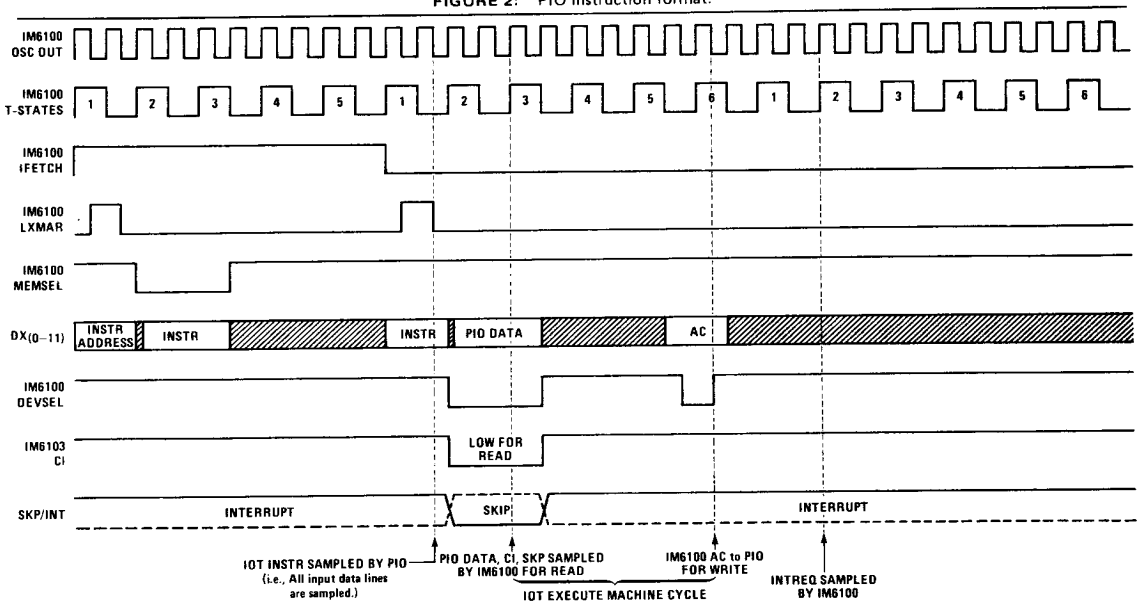
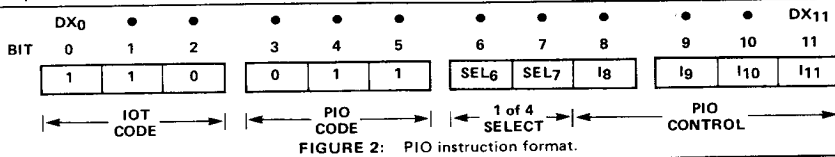
The tristate bidirectional 12-bit DX bus is used to transfer data and control information (Figure 3) between the IM6103 and the IM6100 microprocessor. The IM6100 transmits the device address and control information on the DX bus during the 'execute' phase of an Input-Output Transfer (IOT) instruction. The IM6103 accepts this information on the falling edge of the LXMAR (Address Latch Enable) Signal.

The address bits (6-7) are compared with the chip select inputs (SEL₆ and SEL₇) to address 1 of 4 PIO's. The IOT address bits (3-5) are programmed internally to respond to the bit pattern 011. The SEL₆ and SEL₇ inputs should be externally hard-wired to match the DX₆ and DX₇ chip select bits. As shown in Fig. 3, DEVSEL goes low, during the first half of an IOT execute machine cycle for a read operation and it goes low again in the second half for a write operation. The IM6103 responds to a 'read' instruction by putting data

on the DX bus and C₁ output (of IM6103) low when DEVSEL (from IM6100) input is low. C₁ line goes low to indicate an input transfer cycle to the IM6100. All PIO data transfers to the IM6100 Accumulator (AC) is an 'OR' transfer, (i.e., PIO data is OR'ed into the contents of the AC).

During the write operation into PIO, the PIO accepts data from the IM6100 Accumulator on the rising edge of the DEVSEL. During and after the PIO write, the contents of the accumulator are not cleared.

SKP/INT line goes low during the 'read' DEVSEL if the IM6103 is responding to a 'skip' instruction, and the 'skip' condition is met, therefore causing the IM6100 to skip the next sequential instruction. SKP/INT line reflects the interrupt request status of the IM6100 at all times except during the 'read' DEVSEL. The SKP/INT line goes low if an active interrupt request is pending. During read DEVSEL mode, the SKP/INT indicates the current skip condition. The bits are interpreted as shown below:



OPERATION OF PORT BUFFERS

The IM6103 has 20 I/O pins which can be individually programmed in groups of 4, 8 or 12 bits in three different modes of operation.

In Mode 11, the 20 I/O lines are divided into three ports:
 -Port A with 4 bits (PA₈-PA₁₁)

- Port B with 12 bits (PB₀-PB₁₁)
- Port C with 4 bits (PC₈-PC₁₁)

In Mode 10, the 20 I/O lines are grouped into 2 ports—
 -Port A with 8 bits (PA₄-PA₁₁)
 -Port B with 12 bits (PB₀-PB₁₁)
 -The four I/O lines associated with Port C in Mode 11 (PC₈-PC₁₁) are allocated to Port A as PA₄-PA₇.

In Mode OX, there are two ports—Port B with 12 bits and Port C with 4 bits and four lines for handshake control logic. Four lines of Port A in Mode 11 (PA8-PA11) are re-assigned as handshake control lines. They are:

- Input Register Strobe (IRS)
- Input Register Empty (IRE)
- Output Register Strobe (ORS)
- Output Register Empty (ORE)

The handshake logic controls the data transfer for the Port B. Port C operation remains the same as in Mode 11.

For an 'input' transfer in OX Mode, the input register empty (IRE) output goes high to indicate to the peripheral device that the input register is empty (as shown in Fig. 4). The peripheral device may then strobe in the new data into Port B with Input Register Strobe (IRS). At this time, IRE goes low to indicate to the peripheral device that the input buffer is full, and remains low until Port B has been read by the IM6100 microprocessor. IRE then goes high after the IM6100 executes a Read Port B (RPB) instruction to initiate another input sequence. The data into Port B should be valid only for a short duration before and after IRS makes the 1 to 0 transition.

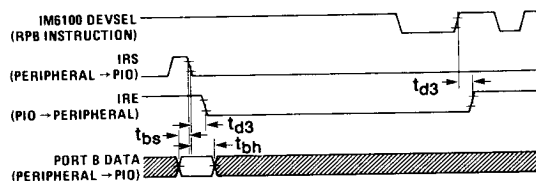


FIGURE 4: Input data transfer (peripheral device to PIO).

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For an 'output' transfer in OX mode, the IM6100 microprocessor writes the data into Port B and its timing is shown in Figure 5. ORF line from the PIO goes high, signaling the peripheral device that the output register is full. The peripheral device may then strobe in the new data from Port B with ORS. Port B stays in the high impedance mode until ORS is activated by the peripheral device. ORF line goes low and remains low until Port B has been written into by the IM6100 microprocessor. ORF then goes high, initiating another output sequence.

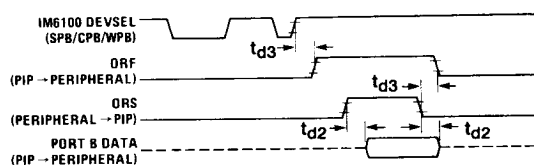


FIGURE 5: Output data transfer (PIO to peripheral device).

The IM6100 monitors the status of ORF (Output Register Full). If it is low (i.e., output register is empty), IM6100 may load data into Port B output buffer with SPB/CPB/WPB instruction. ORF goes high a delay time after the rising edge of the 'write' DEVSEL, signaling the peripheral device that output buffer has new data. During this time, Port B output buffers remain tristated. The peripheral device may then enable and read out Port B output latches by activating ORS (Output Register Strobe) high. The falling edge of ORS (from high to low) signals the PIO that the peripheral device no longer needs the valid current information. Port B is tristated and ORF then goes low, thereafter, to indicate another output sequence.

ORF should be set to 0 and IRE to 1 with a 'write' command in Mode OX, to initiate the handshaking sequence.

The IM6100 microprocessor should not write into Port B until ORF is low for an 'output' transfer and should not read Port B until IRE is low for an 'input' transfer. The peripheral device reads Port B if ORF is high and writes into Port B if IRE is high.

The PIO may be programmed to generate an INTREQ (Interrupt Request) to the microprocessor when ORF or IRE goes low by setting the respective Interrupt enable bits, OREN and IREN.

The IM6100 may poll the status of ORF or IRE by executing the respective skip instructions SKPOR and SKPIR, by reading the status register or by reading "Port A".

In Mode 11 and 10, when handshaking control is not in effect, the execution of SKPOR and SKPIR Instructions depend on the state of the Port A lines PA11 and PA8, respectively. The Interrupt feature is available only in Mode OX.

The mode of operation — 11, 10 or OX, is selected by programming the Status Register (SR).

All ports are bidirectional. The execution of a 'write' instruction caused a port to be automatically programmed to be an 'output'. The output data may be changed by using the 'set', 'clear' or 'write' instructions. The output remains valid until the port bit lines are reset to be inputs.

Execution of a 'read' instruction causes a port to be automatically set as an 'input' port — i.e., it presents a very high impedance to the I/O lines. Data appearing on the I/O lines will be sampled into the port input latch at every LXMAR pulse and may be read by the IM6100 microprocessor by the 'read' instruction.

In Mode OX, Port B acts as a tristate bidirectional buffer which is controlled by an external peripheral device. ORF and IRE lines are outputs and ORS and IRS lines are inputs.

At power-on, all ports are defined to be input ports and the PIO is initialized to be in Mode 10. With 20 I/O lines partitioned into the 8/12 (i.e., Port A = 8 bits, Port B = 12 bits) format.

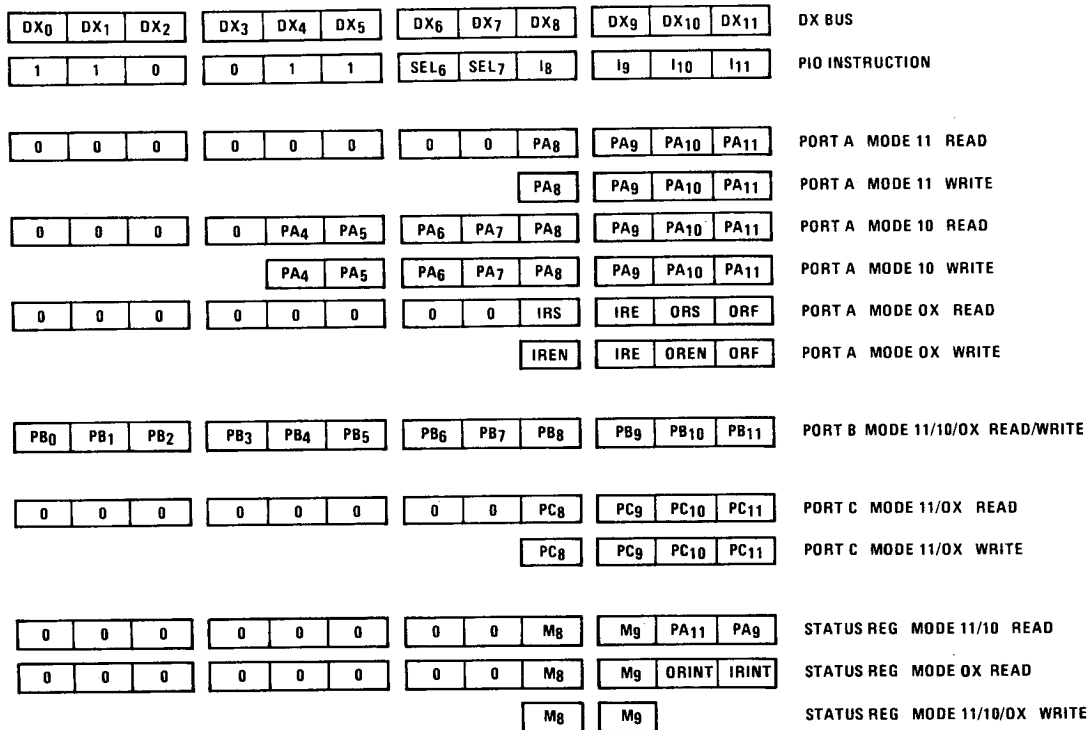


FIGURE 6: IM6103 PIO register bit assignments.

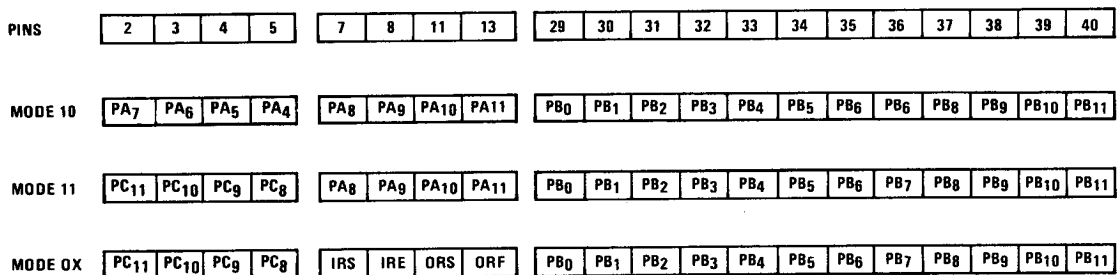


FIGURE 7: IM6103 PIO port pin assignments.

IM6103

PIO INSTRUCTION

NOTE: Symbol Definition — “•” — AND
 “+” — OR
 “=” — Is Replaced By

PIO CONTROL	MNEMONICS	DESCRIPTION
0 0 0 0	SETPA (Set Port A)	Set PA_i to 1 if AC_i is 1. AC is not cleared. Mode 11: $PA_i = PA_i + AC_i$, $8 \leq i \leq 11$ Mode 10: $PA_i = PA_i + AC_i$, $4 \leq i \leq 11$ Mode OX: $IREN = IREN + AC_8$ $IRE = IRE + AC_9$ $OREN = OREN + AC_{10}$ $ORF = ORF + AC_{11}$
0 0 0 1	CLRPA	Clear Port A. Clear PA_i to 0 if AC_i is 1. AC is not cleared. Mode 11: $PA_i = PA_i \cdot \overline{AC_i}$, $8 \leq i \leq 11$ Mode 10: $PA_i = PA_i \cdot \overline{AC_i}$, $4 \leq i \leq 11$ Mode OX: $IREN = IREN \cdot \overline{AC_8}$ $IRE = IRE \cdot \overline{AC_9}$ $OREN = OREN \cdot \overline{AC_{10}}$ $ORF = ORF \cdot \overline{AC_{11}}$
0 0 1 0	WPA	Write Port A. Set PA_i equal to AC_i . AC is not cleared. Mode 11: $PA_i = AC_i$, $8 \leq i \leq 11$ Mode 10: $PA_i = AC_i$, $4 \leq i \leq 11$ Mode OX: $IREN = AC_8$ $IRE = AC_9$ $OREN = AC_{10}$ $ORF = AC_{11}$
0 0 1 1	RPA	Read Port A. ‘OR’ transfer PA to AC. Mode 11: $AC_i = AC_i + PA_i$, $8 \leq i \leq 11$ $AC_i = AC_i$, $0 \leq i \leq 7$ Mode 10: $AC_i = AC_i + PA_i$, $4 \leq i \leq 11$ $AC_i = AC_i$, $0 \leq i \leq 3$ Mode OX: $AC_8 = AC_8 + IRE$ $AC_9 = AC_9 + IRE$ $AC_{10} = AC_{10} + ORS$ $AC_{11} = AC_{11} + ORF$ $AC_i = AC_i$, $0 \leq i \leq 7$
0 1 0 0	SETPB	Set Port B. Set PB_i to 1 if AC_i is 1. AC is not cleared. $PB_i = PB_i + AC_i$, $0 \leq i \leq 11$
0 1 0 1	CLRPB	Clear Port B. Clear PB_i to 0 if AC_i is 1. AC is not cleared. $PB_i = PB_i \cdot \overline{AC_i}$, $0 \leq i \leq 11$
0 1 1 0	WPB	Write Port B. Set PB_i equal to AC_i . AC is not cleared. $PB_i = AC_i$, $0 \leq i \leq 11$

PIO CONTROL	MNEMONICS	DESCRIPTION
0 1 1 1	RPB	Read Port B. ‘OR’ transfer PB to AC. $AC_i = AC_i + PB_i$, $0 \leq i \leq 11$
1 0 0 0	SETPC	Set Port C. Set PC_i to 1 if AC_i is 1. AC is not cleared. Mode 11 and OX: $PC_i = PC_i + AC_i$, $8 \leq i \leq 11$ Mode 10: No operation
1 0 0 1	CLRPC	Clear Port C. Clear PC_i to 0 if AC_i is 1. AC is not cleared. Mode 11 and OX: $PC_i = PC_i \cdot \overline{AC_i}$, $8 \leq i \leq 11$ Mode 10: No operation
1 0 1 0	WPC	Write Port C. Set PC_i equal to AC_i . AC is not cleared. Mode 11 and OX: $PC_i = AC_i$, $8 \leq i \leq 11$ Mode 10: No operation
1 0 1 1	RPC	Read Port C. ‘OR’ transfer PC to AC. Mode 11 and OX: $AC_i = AC_i + PC_i$, $8 \leq i \leq 11$ Mode 10: No operation
1 1 0 0	SKPOR	Skip the next sequential instruction if PA_{11}/ORF is low. Mode 11 and 10: Skip if PA_{11} is low. Mode OX: Skip if ORF is low.
1 1 0 1	SKPIR	Skip the next sequential instruction if PA_9/IRE is low. Mode 11 and 10: Skip if PA_9 is low. Mode OX: Skip if IRE is low.
1 1 1 0	WSR	Write Status Register. AC is not cleared. $M_8 = AC_8$ $M_9 = AC_9$
1 1 1 1	RSR	Read Status Register. ‘OR’ transfer Status register to AC. $AC_8 = AC_8 + M_8$ $AC_9 = AC_9 + M_9$ $AC_i = AC_i$, $0 \leq i \leq 7$ Mode 11 and 10: $AC_{10} = AC_{10} + PA_{11}$ $AC_{11} = AC_{11} + PA_9$ Mode OX: $AC_{10} = AC_{10} + ORINT$ $AC_{11} = AC_{11} + IRINT$

STATUS REGISTER

The Status Register (SR) has 2 mode bits, M_8 and M_9 which can be modified by the WSR (Write Status Register) instruction. These two bits define the mode of operation for the IM6103 as shown in Figure 8.

M_8	M_9	MODE	PORT OPERATION
0	*	Mode OX	PB0-11, PC8-11, IRS, IRE, ORS, ORF
1	0	Mode 10	PB0-11, PA4-11
1	1	Mode 11	PB0-11, PC8-11, PA8-11

FIGURE 8: Mode bit assignments.

The Mode and Interrupt status bits, ORINT (Output Register empty Interrupt) and IRINT (Input Register empty Interrupt), may be read with the RSR (Read Status Register) instruction. The interrupt status bits are set to 0 if the corresponding flag is requesting an interrupt.

In Mode 11/10 the current value of PA_{11} and PA_9 can be interrogated. In this mode, Port A can be either an input or an output. M_8 and M_9 are initialized to "11" at power-on.

DX_8	DX_9	DX_{10}	DX_{11}	DX	BUS
M_8	M_9	ORINT	IRINT	SR	MODE OX READ
M_8	M_9	PA_{11}	PA_9	SR	MODE 11/10 READ
M_8	M_9			SR	MODE 11/10/OX WRITE

FIGURE 9: Status register bit assignments.

SKIP OPERATION

The IM6100 may poll the status of ORF or IRE in Mode OX, by executing a skip instruction, SKPOR or SKPIR. The IM6103 will assert the SKP/INT line low if the corresponding status line (ORF or IRE) is low, causing the next sequential instruction to be skipped. During this cycle, ORF and IRE remain unchanged.

In Mode 11/10, SKPOR and SKPIR instruction executions depend on the state of PA_{11} and PA_9 , respectively. Port A may be an input or output port.

If ORF is reset to 0 by executing a CLRPA or WPA instruction to initiate the handshaking sequence, the next SKPOR instruction will cause the next sequential instruction to be skipped.

INTERRUPT OPERATION

The IM6103 may be programmed to generate an interrupt request input (INTREQ) when ORF or IRE goes low, by setting the corresponding interrupt enable bits, OREN or IREN, to 1. If the IM6100 interrupt system has been previously enabled, the microprocessor will acknowledge the INTREQ input. If the IM6100 μP does not see the higher priority INTREQ's, inputs from other peripheral controllers such as IM6102 Memory Extender/Direct Memory Access/Internal Timer Controller (MEDIC) or IM6101 Parallel Interface Elements (PIE) in the system, the interrupt service routine should initiate a software poll of the PIO's in the system to identify the particular PIO that generated the INTREQ. In Mode OX, the interrupt request status of ORF and IRE may be identified by reading the Status Register. ORINT or IRINT will be set to 0 if ORF (being low) or IRE (being low) is generating an INTREQ. Note that IM6102 MEDIC and IM6101 PIE provide an automatic priority vectoring.

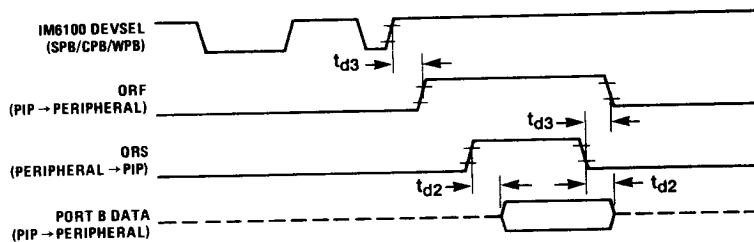
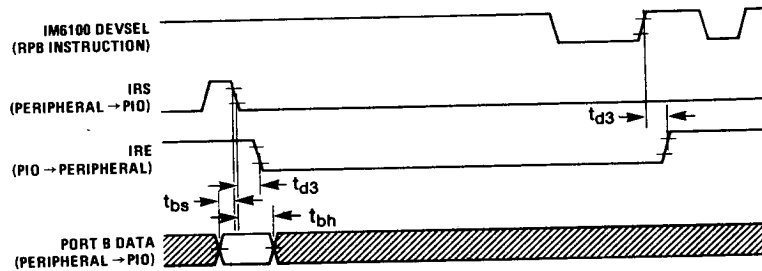
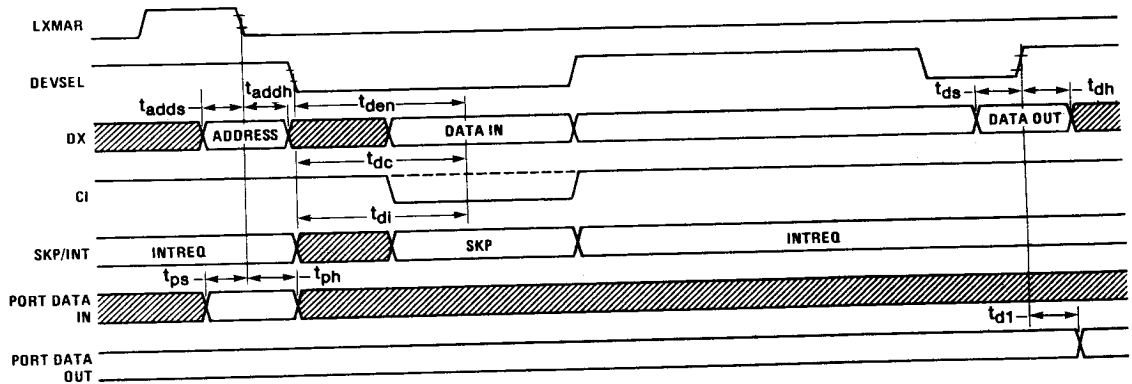
The interrupt feature of IM6103 is available only in Mode OX. An ORF INTREQ may be removed by one of the following methods:

- executing a SPB/CPB/WPB Instruction (ORF goes high if Port B is written into), or
- setting ORF to 1 with SPA/WPA Instruction, or
- by resetting OREN to 0 with a CPA/WPA Instruction, or
- by changing to Mode 11/10.

An IRE INTREQ may be removed by:

- executing a RPB Instruction (IRE goes high after Port B is read), or
- setting IRE to 1 with SPA/WPA Instructions, or
- resetting IREN to 0 with a CPA/WPA Instruction, or
- changing to Mode 11/10.

PIO may be software programmed to generate an INTREQ to the IM6100 by resetting ORF or IRE to 0 with a CPA/WPA Instruction and by setting the corresponding enable bit, OREN or IREN, with a SPA/WPA Instruction in Mode OX.

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APPLICATION OF IM6103

Figure 13 illustrates a microcomputer system block diagram using IM6103 in a dual processor system.

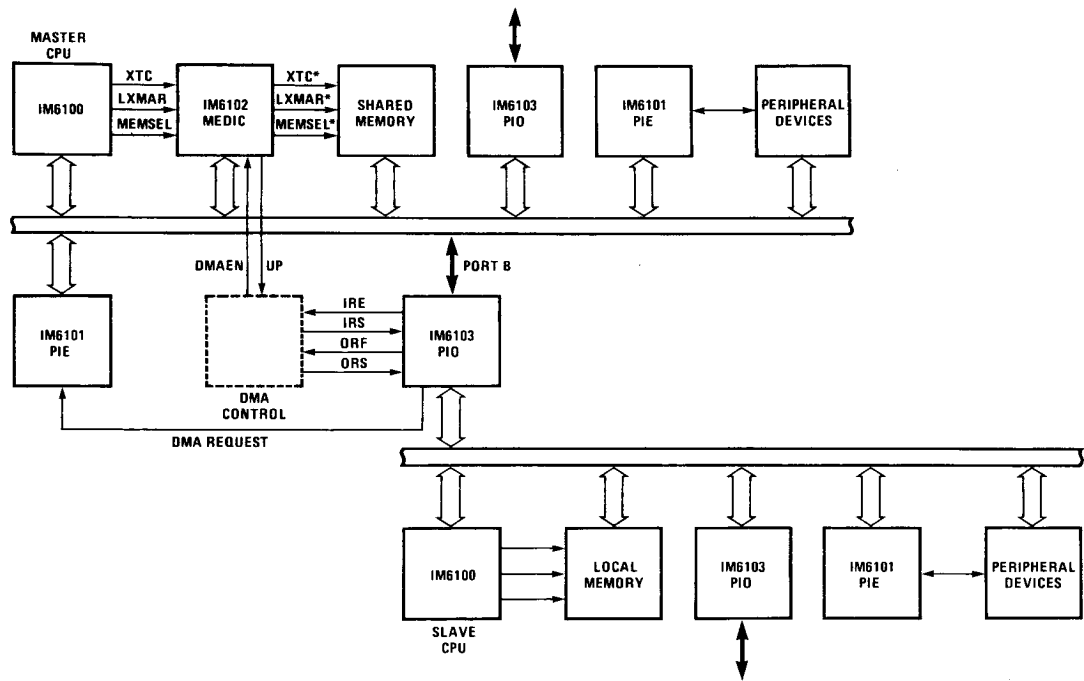


FIGURE 13: Dual processor system with shared memory.